A Deterministic Dynamic Element Matching Approach for Testing High-Resolution ADCs With Low-Accuracy Excitations

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***Abstract*—Dynamic element matching (DEM) is capable of providing good average linearity performance in matching critical circuits in the presence of major component mismatch, but the approach has received minimal industrial adoption outside of $\Sigma-\Delta$ structures because of challenges associated with implementation of a required randomizer and because of the time-local nonstationarity. This paper presents a DEM approach to analog-to-digital converter (ADC) testing in which low-precision DEM digital-to-analog converters (DACs) are used to generate stimulus signals for ADCs under test. It is shown that in a testing environment, this approach provides very high precision test results, and time-local nonstationarity is of no concern. In addition to traditional random DEM techniques, a deterministic DEM (DDEM) strategy that eliminates the need for a randomizer is introduced. The performance of the DDEM method is established mathematically and validated with detailed simulation results. Furthermore, the DDEM method requires far fewer samples to achieve the same level of average linearity than the random DEM approach. It is demonstrated that both the random DEM and DDEM methods can be used to accurately test ADCs with linearity that far exceeds that of the DAC used as a signal generator. This technique of using imprecise excitations and DEM to test much more accurate ADCs offers potential for use in both production test and built-in self-test environments where high linearity test sources are difficult to implement.**

***Index Terms*—Analog-to-digital converter (ADC) testing, built-in self-test (BIST), dynamic element matching (DEM), integral nonlinearity (INL) testing.**

I. Introduction

THE International Technology Roadmap for Semiconductors (ITRS) [1] recognizes analog-to-digital converters (ADCs) as the world's largest volume mixed-signal circuits. With the increasing complexity of mixed-signal circuits and the growing market opportunities for low-cost mixed-signal integrated circuits (ICs), testing of analog and mixed-signal circuits in general and ADCs in particular has become a challenging and costly process [2]. Long test times and the large investments required for the commercial mixed-signal testers needed to test high-performance parts with existing test flows have created a large demand for alternative cost-effective testing strategies. Built-in self-test (BIST) structures for analog and mixed-signal circuits are widely recognized as a potential testing alternative for not only reducing costs associated with using production testers but also providing a capability to test deeply embedded systems on a chip (SOCs). BIST approaches can also provide value added and performance enhancement if incorporated with self-calibration functionality [3]. There have been numerous attempts to provide BIST solutions for ADCs, and most approaches in the literature [4]–[11] have concentrated on duplicating the operation or performance of a standard tester on-chip. To date, these methods have received little industrial adoption. With no practical BIST solution to this and related analog and mixed-signal problems on the horizon, the authors of the 2001 ITRS stated that designs for test and BIST for analog and mixed-signal circuits are essentially unsolved [1].

In the conventional approach to testing ADCs, a highly accurate signal is used to stimulate the device under test (DUT). This stimulus input is typically generated by a digital-to-analog converter (DAC) with substantially higher precision than that of the DUT. In duplicating the production testing strategy, most BIST approaches in the literature also require signal generators that have substantially higher resolution and linearity than the DUT. This presents a major design challenge because such high-performance signal generators invariably require more design effort and more silicon area than the ADC to be tested.

A new approach to accurately testing an ADC in a production or BIST environment with dramatically reduced accuracy requirements on the test signal generator was recently introduced [3], [12]–[14]. With this approach, signal-processing techniques are used to accurately extract performance characteristics of the DUT that are embedded in output test data generated with low-accuracy signal generators. In [3], a test algorithm was developed that takes advantage of inherent redundancy in two nonlinear input signals to accurately test ADCs. In [12], a test algorithm incorporated information about the spatial frequency separation of the nonlinear input spectrum from that of the DUT to characterize an ADC to accuracies that far exceed the linearity of the stimulus. The mathematics behind linearity testing of ADCs using nonlinear test signals unknown to the test algorithm is presented in [13], where a nonlinear stationary excitation and a level-shifted version of the nonlinear excitation

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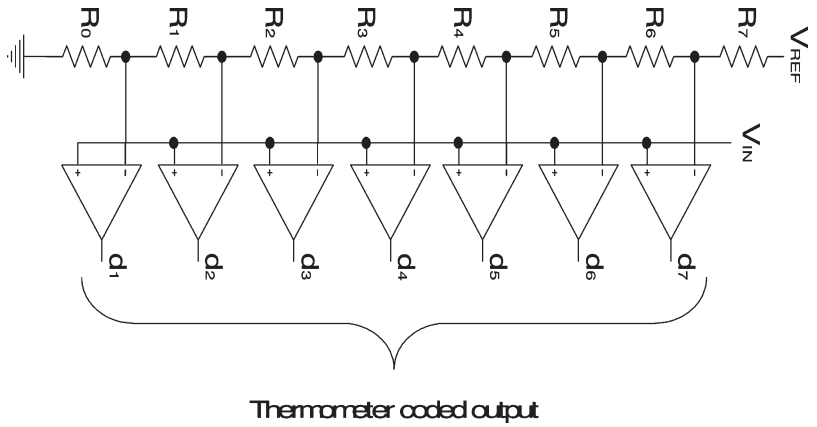

Fig. 1. Three-bit flash ADC.

are used as inputs to the DUT. Simulations and experimental results were used to validate this approach [13], [14].

In this paper, we will present an alternative approach to testing ADCs using low-accuracy DACs along with dynamic element matching (DEM) techniques to achieve very high accuracy in the testing of an ADC. By a low-accuracy DAC, we mean a DAC implemented on-chip within a small die area requiring low design effort. Such a DAC serves as a very low cost signal source, but at the same time, it will have low linearity and low precision. In the rest of the paper, we will use these terms interchangeably when describing such a DAC. In contrast to the referenced work on using nonlinear sources along with specialized signal-processing algorithms to characterize the DUT, the approach presented here can utilize existing code-density-based algorithms for processing test data generated at the output of the ADC under test.

A discussion of how the ADC to be tested is modeled and how the integral nonlinearity (INL) is calculated is given in Section II. The concepts of DEM are discussed in Section III. Details of using both random DEM and DDEM for test signal generation are presented in Section IV. In Section V, simulation results for using DDEM for testing high-resolution ADCs are discussed. A mathematical formulation of signal generation for ADC testing using the DDEM approach is provided in Section VI.

II. ADC Model and INL Calculation

Although the proposed DEM methods for generating stimulus signals can be used to test any type of ADCs, this paper will focus on flash ADC testing. This focus will be followed because we believe that linearity testing of a flash ADC is modestly more challenging than testing of other ADC types due to the random nature of all transition voltages (breakpoints) of the flash ADC. Extension of the concept to other ADC architectures is straightforward.

The architecture for the flash ADC that will be used to represent the DUT is the basic structure depicted (for 3-bit resolution) in Fig. 1. Not shown is a thermometer to binary converter that converts the thermometer-coded output of the comparators to a binary output. When an unknown input voltage is presented to the ADC, the ADC outputs a binary code that is equal to the

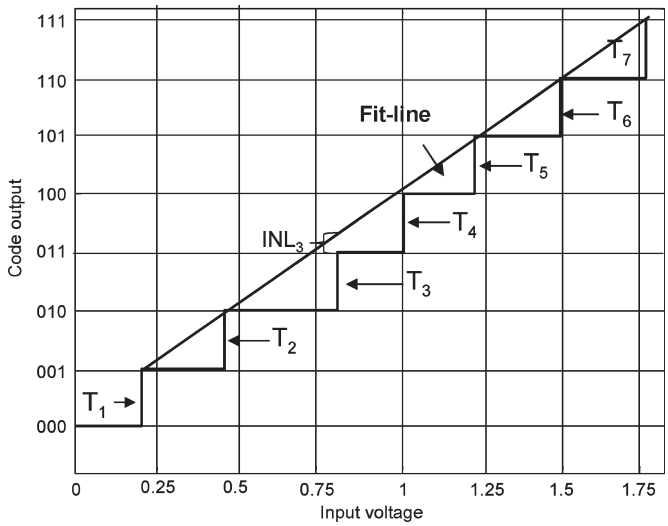

Fig. 2. Nonideal ADC transfer curve and its fit line.

number of comparators triggered. The relationship between the ADC output code and the input voltage is referred to as the ADC's transfer curve as shown by the staircase curve in Fig. 2. In an ideal flash ADC, the tap voltages in the resistor string are uniformly spaced, and the comparators have no offset voltages, resulting in uniformly spaced transition voltages. In this case, the staircase curve will have all the step edges lying perfectly on a straight line, and one would have a perfectly linear ADC.

In an actual ADC, the transition voltages will differ from their ideal values due to both resistor mismatches and comparator offsets as a result of process variations. Although the effect of process variations may appear random from batch to batch, from wafer to wafer, from die to die, or even from one local area to another on the same die, their total effect to the ADC's transfer curve is fixed once the ADC is fabricated. This effect causes the step edges in the transfer curve to move away from the straight line, resulting in a nonlinear transfer curve. This transfer curve nonlinearity is termed the ADC's static nonlinearity and is characterized, in part, by the INL and differential nonlinearity (DNL) performance specifications of an ADC. The effects of the random components of the transition voltages can be seen in a typical transfer characteristics of an ADC shown in Fig. 2 for $V_{\mathrm{REF}} = 2$ V.

There are several alternative but similar definitions of the INL of an ADC. Some authors [15] define an INL function as a continuous function of the ADC input voltage INL(Vin). Others define an INL function from a discrete sequence denoted as INL_k determined by the transition points of the ADC, and others define an INL function from a discrete sequence of output code densities obtained by exciting the ADC with a known test signal such as a ramp or sinusoid. In all cases, the INL is defined to be the maximum magnitude of either the continuous or discrete INL functions, and in all cases, there is usually not much difference in the INL obtained from any of the three definitions. In this paper, we follow what is most commonly used by test engineers in industry in defining the INL. Specifically, the transition point T_k will be first estimated from code density outputs of the DUT generated from a characterized input signal. The INL_k of an ADC is defined relative to a fit line to the actual transfer characteristics. The fit line is usually the endpoint fit line and is depicted in Fig. 2. If we define n to be the resolution of the ADC and let $N = 2^n$, an ideal n-bit ADC will have $N-1$ uniformly spaced transition points. If there are no missing codes in the ADC output, the nonideal ADC will have transition points at $T_1, T_2, \ldots, T_{N-1}$. The $N-1$ uniformly spaced points on the endpoint fit line are denoted by $\underline{T_1}, \underline{T_2}, \ldots, \underline{T_{N-1}}$ and are related to the actual first and last transition points by the expression

$$\underline{T_k} = T_1 + \frac{T_{N-1} - T_1}{N-2}(k-1), \qquad k = 1, 2, \ldots, N-1. \tag{1}$$

The pairwise difference between the actual transition points and the fit-line transition points is defined as INL_k and is expressed in LSBs as

$$\mathrm{INL}_k = \frac{T_k - \underline{T_k}}{1\mathrm{LSB}} = \frac{T_k - T_1}{T_{N-1} - T_1}(N-2) - (k-1) \qquad k = 1, 2, \ldots, N-1. \tag{2}$$

Since the fit line is the endpoint fit line, $\mathrm{INL}_1 = \mathrm{INL}_{N-1} = 0$.

A linear ramp is widely used in industry as the input signal, and the numbers of occurrences of each output are tallied into corresponding code bins. Notationally, H_k is the number of occurrences of code k, and the accumulated code density to code k, H_{ck} is given by the expression

$$H_{ck} = \sum_{i=1}^{k} H_i. \tag{3}$$

Since V_{in} is proportional to time and the sampling intervals are constant, the total number of accumulated samples for a linear ramp input is linearly proportional to V_{in}. Thus, the transition voltages can be estimated from the corresponding code densities and from these estimates, an estimate of INL_k as given in (2) can be expressed as

$$\mathrm{INL}_k \cong \overline{\mathrm{INL}_k} = \frac{H_k - H_1}{H_{N-1} - H_1}(N-2) - (k-1) \qquad k = 1, 2, \ldots, N-1. \tag{4}$$

Tests using $\overline{\mathrm{INL}_k}$ as the measured value of INL_k are often termed histogram-based tests, and the histogram-based method is widely used to test ADCs. For the code density estimate $\overline{\mathrm{INL}_k}$ to provide a good estimate of INL_k, it is imperative that the linearity of the input ramp be a decade or more better than that desired of the ADC under test because any nonlinearity in the input signal will be directly translated into INL_k estimation errors with the histogram method. Thus, if the ramp is generated using a DAC, the DAC must have resolution and linearity that are at least 3 bits higher than the targeted resolution and linearity of the DUT. This is a major challenge in production testing of high-resolution ADCs and an even greater challenge for BIST solutions of both medium- and high-resolution ADCs.

The DEM histogram-based testing method discussed in this paper overcomes this challenge by allowing the use of low-linearity DACs for high-accuracy testing of ADCs. With the DEM approach, the same signal-processing algorithms used in the histogram method are used to "measure" the ADC linearity performance. This is possible because the histogram data generated with DEM DACs is, in an appropriate statistical sense, nearly identical to the histogram data that would be generated if an ideal linear ramp were used to test the ADC.

III. DEM

The performance of most useful DAC architectures is dependent upon the matching properties of a set of critical circuit elements. Depending on the architecture, these elements might be resistors, capacitors, or transistors. Element-matching errors are inevitable due to inherent process variations. Special layout techniques are widely used to reduce these errors, but layout alone cannot provide the matching performance needed for obtaining an acceptable yield in many applications. Increases in area, special processes, and/or laser trimming can be used to further reduce the effects of matching errors, but these methods generally come at the expense of significant cost increases, thus limiting where these approaches are economically viable.

The DEM approach [16], [17], introduced by Van De Plassche in 1976, is based upon dynamically rearranging matching critical elements so that, in a statistical time-average sense, the circuit performs as if the elements were matched. In some applications, good statistical time-average matching performance provides the same system performance as would be obtained if actual matching were achieved, and in others, the local nonstationarity inherent with DEM is totally unacceptable. Standard linearity performance specifications such as INL and DNL are often defined in the context of a static transfer characteristic of a device but measured by taking a large number of samples and using various signal-processing algorithms to extract these linearity specifications from a large set of measurement data. This approach to measuring key performance specifications can mask the local nonstationarity inherent with DEM structures.

The DEM method was used by Jensen and Galton [18], [19] to improve linearity performance of DACs. In particular, they showed that DEM can appreciably improve the spurious-free dynamic range (SFDR) performance of moderately low-linearity DACs [18]. The improvement in linearity

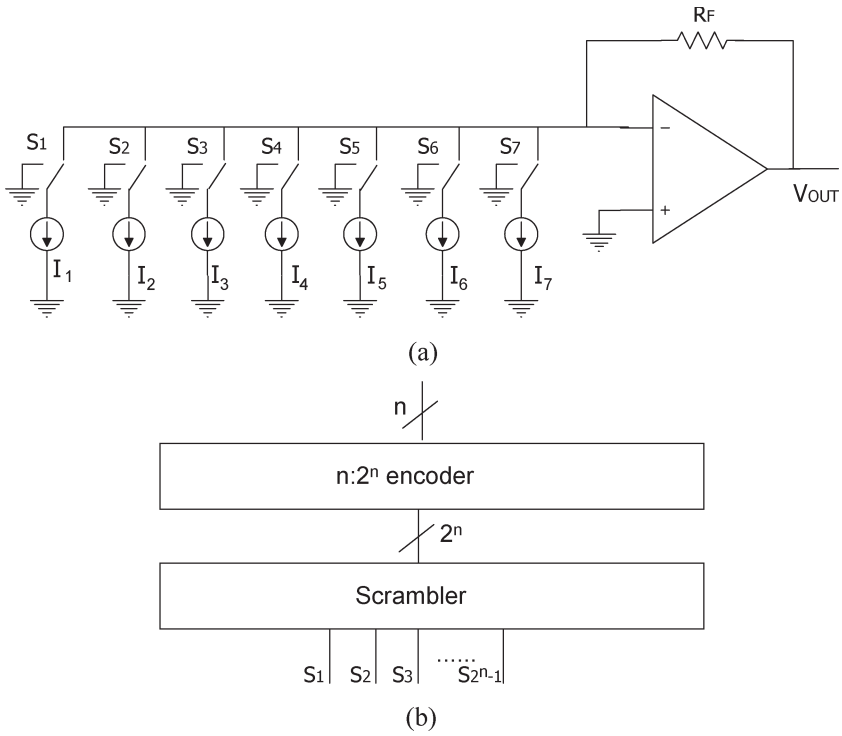

Fig. 3. (a) Three-bit current mode thermometer-coded DEM DAC. (b) DEM switching signals generator.

specifications is attributable to the randomizing effect provided by DEM, which spreads errors in the DAC over a wide frequency spectrum. Although this approach provides a significant improvement in a linearity specification if a large number of output samples is used to characterize the DAC, DEM does not reduce the errors in individual DAC output voltage samples, nor does it reduce the errors in the average values if a short observation time window is used. These instantaneous or short time-average errors are termed time-local errors of the DAC, and they significantly limit the applications of DEM. Other researchers [20]–[27] have used DEM in $\Delta-\Sigma$ converters, and the high oversampling ratio inherent in these structures can either partially or totally remove the limitations associated with the time-local errors. Most of these algorithms are input data-dependent and are based upon variants of a "first use–next use" algorithm. A first use–next use algorithm tries to use all or most elements before reusing them, and when reuse occurs, those used next will be the ones that were previously used first, much like the data flow in and out of a first-in first-out (FIFO) memory structure. Included in these data-dependant first use–next use (DDFN) algorithms are what some authors term individual level averaging (ILA) [20], data weighted averaging (DWA) [21], and some variations [22]–[25] of these approaches.

Although there are limitations of where DEM-based DACs with a good "linearity specification" can be used because the actual nonlinearity is not removed, the improved linearity specification provided by DEM can be exploited if DEM DACs are used to generate stimulus signals for ADC testing. This approach is particularly attractive for BIST applications because a DEM test signal generator can be realized with a not-so-accurate DAC, thus dramatically reducing the silicon area and design overhead needed for including BIST circuitry on chip.

In this paper, two types of component switching sequences are used to improve the effective linearity of a DAC used to test an ADC. One is a standard DEM approach, and the other uses a deterministic switching sequence to derive a desired mean performance of a DAC. We will call the latter approach a deterministic DEM (DDEM) approach. To distinguish between the random and deterministic switching sequences used for DEM, we will use the term "random DEM" when particular emphasis on the random nature of a switching sequence is needed.

In the DEM approaches discussed in this paper, the DEM DAC may have nominally more physical bits of resolution than the ADC under test, or it may have comparable resolution but the inherent linearity requirements of the DAC will be several bits less than that of the DUT. Although the DEM approach can be used for testing several performance parameters of an ADC, in this work, we will restrict the focus to testing the INL performance of an ADC.

IV. DEM DACS FOR ADC TESTING

A current-steering thermometer-coded DAC is shown in Fig. 3(a). Ideally, all current sources are of the same value and all switches are matched. If the operational amplifier (op amp) has sufficiently high gain or is sufficiently linear, the output of the DAC will be linearly related to the digital input code if a simple binary to thermometer $n : 2^n$ decoder is used to drive the switches. If there is mismatch in the current sources, however, there will be a nonlinear relationship between the digital input code and the resultant analog output of the DAC. The current-steering DAC of Fig. 3(a) can be converted to a DEM DAC if a randomizer (sometimes termed a scrambler) is placed between

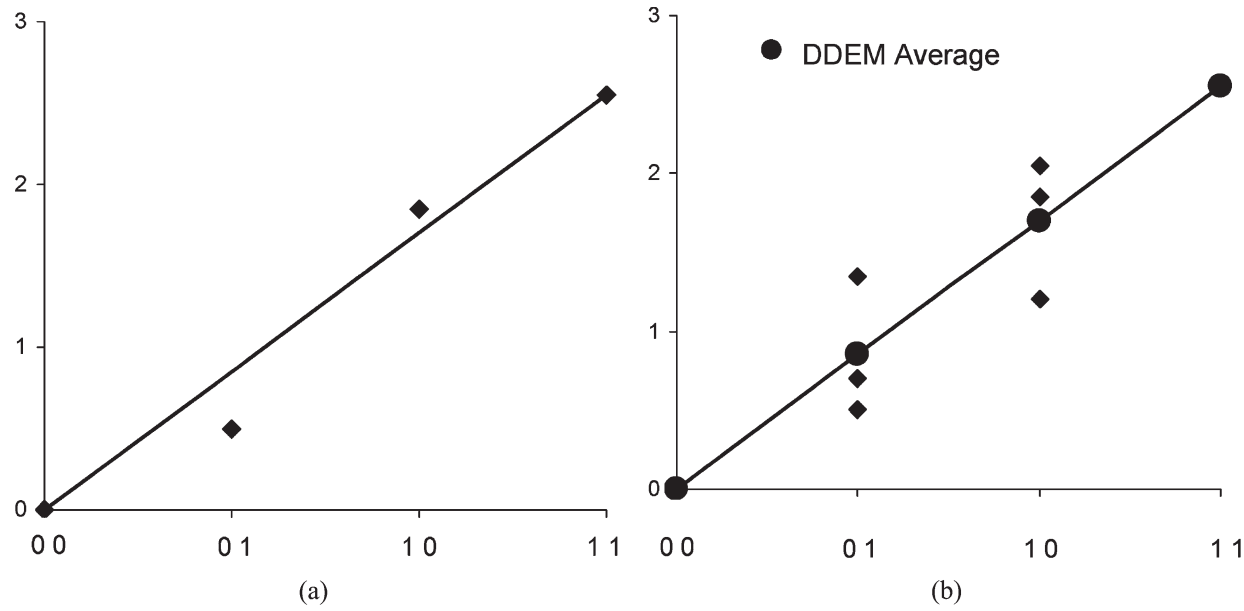

Fig. 4. Two-bit current-steering DAC example.

the $n : 2^n$ encoder and the switches of the DAC, as shown in Fig. 3(b). With an ideal randomizer, every time any input code k is presented to the randomizer, it will randomly select and turn on k switches. In this way, the expected value of the output current will be proportional to k for all input codes. If the op amp introduces no nonlinearities, the expected output of the DAC is linearly related to the input code, and thus, if a sufficiently large number of samples are used to measure linearity properties of the DAC such as INL, total harmonic distortion (THD), or SFDR, the DEM DAC will have measured properties that agree with those of a truly linear DAC, but individual outputs of the DAC or outputs over short time intervals of the DAC can be far from linear. If the intrinsic nonlinearity of the DAC is m bits lower than the physical resolution of the DAC, short-term deviations from a linear fit line can be in excess of 2^m bits, and short-term differential nonlinearities can be even larger. This short-term nonstationarity is an unavoidable and inherent limitation of DEM DACs and limits where they can be used. Even in applications where the nonstationarity is not a problem, the issue of the randomizer does present some challenges, and a major portion of the research on using DEM has been focused on the randomizer. If the randomizer does not provide a purely random output, spectral tones will appear in the DAC output, and these tones are unacceptable in many applications. Invariably two issues must be simultaneously addressed when designing the randomizer. One is the randomness of the output, and the other is the hardware complexity needed to select the switches identified by the randomizer. It is these tradeoffs that most researchers have focused on. Short-length deterministic switching sequences are particularly attractive because the hardware requirements for implementing these switching sequences can be very small, but the spectral tone problem can be severe, and most short-length and even intermediate-length deterministic switching sequences will not provide an output on a chip that is average linear. Some deterministic switching sequences do, however, exist that are perfectly average linear, and some short-length deterministic switching sequences do exist that are nearly average linear, and when a DDEM DAC is used to test an ADC, the concept of tones plays no role on INL testing. Furthermore, with the appropriate deterministic switching sequences, the performance of the DDEM DAC can be much better than that of a random DEM DAC.

The relative performance of a DDEM DAC and a random DEM DAC can be illustrated. Consider a 2-bit current-steering DAC with current sources of values $I_0 = 0$, $I_1 = 0.5$, $I_2 = 1.35$, and $I_3 = 0.7$. The outputs of this DAC along with an endpoint fit line are shown in Fig. 4(a). The current sources in this example are far from matched, and a significant INL should be apparent from Fig. 4(a). Consider now the deterministic switching sequence comprised of exactly three samples per code where for code "00," I_0 is selected three times; where for code "01," I_1, I_2, and I_3 are all selected exactly once; where for code "10," $I_1 + I_2$, $I_1 + I_3$, and $I_2 + I_3$ are each selected once; and where for code "11," $I_1 + I_2 + I_3$ is selected three times. These samples are shown by the diamonds in Fig. 4(b). It should be apparent that all of the intermediate samples deviate substantially from the fit line. The average of the three samples is also shown in the figure. These averages are all exactly on the fit line. Thus, this deterministic switching sequence provides precisely average linear performance. If the deterministic switching sequence length were decreased to two or increased to four, the average for the switching sequence would be far from average linear. This precisely average linear property is not dependent upon the values of the current source, and as will be seen later, this precisely average linear property is particularly attractive when using a DDEM DAC to do linearity testing of an ADC.

Consider now a random DEM switching sequence in which p individual current sources are randomly selected and in which p pairs of current sources are randomly selected for the inputs for codes 01 and 10. The endpoint codes 00 and 11 are of no concern. A simulation for $p = 100$ was run, and the average

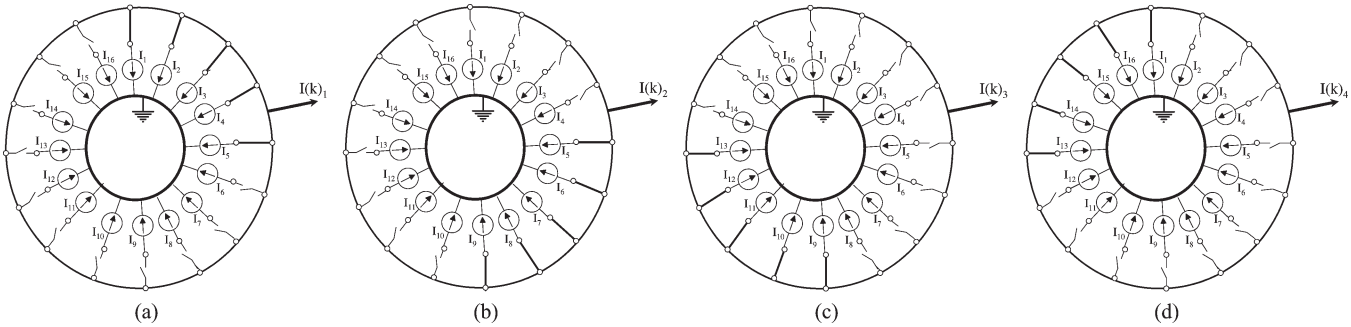

Fig. 5. Cyclic DDEM switching of a 4-bit DAC. (a) First output sample when $k = 5$. (b) Second output sample when $k = 5$. (c) Third output sample when $k = 5$. (d) Fourth output sample when $k = 5$.

value for code 01 was 0.908, and the average value for code 10 was 1.676. These averages deviate by $-.058$ and $+.024$, respectively, from the fit line. Thus, even with 100 samples, the average values deviate from the fit line in contrast to the deterministic switching sequence of length 3, where the average values were precisely on the fit line. This simple example should support the premise that some deterministic switching sequences can be guaranteed to be precisely on the fit line, that some deterministic switching sequences will deviate significantly from the fit line, and that to get close to the fit line in the average sense, a large number of random samples will be required.

A. Natural DDEM Switching Sequence

Consider now the testing of an m-bit ADC with an n-bit DAC. Assume p samples per DAC code are used to generate test signals for the ADC. This would correspond to $n_c = p2^{n-m}$ samples per ADC code. The simple three-element deterministic switching sequence used for the 2-bit example can be extended to any number of bits while still maintaining perfectly linear average performance. We will refer to this as the natural DDEM switching sequence. Implementation of the natural DDEM switching sequence will require $2^n - 1$ excitations for each DAC input code and correspondingly provide, on the average, $2^{n-m}(2^n - 1)$ ADC outputs per ADC output code. For example, testing a 10-bit ADC with a 13-bit DDEM DAC would require 8184 samples/code, and testing a 16-bit ADC with a 19-bit DAC would require 524 280 samples/ADC output code. This high average number of samples per ADC output code is unacceptably high. An alternative deterministic switching sequence will now be described that provides good average linearity performance with a reduced number of samples per ADC output code.

B. Cyclic DDEM Switching Sequence

For convenience, one more current source element has been added to the DAC in Fig. 3; thus, the DAC now has totally $N = 2^n$ current sources. The integer q is defined by the expression $q = N/p$, where it is assumed that p, the number of samples per DAC input code, is selected so that q is an integer.

All current sources are arranged conceptually and sequentially around a circle to visualize a wrapping effect whereby the Nth current source is adjacent to the first current source. The physical layout of the current sources does not need to have any geometric association with this cyclic visualization.

1) Define p index current sources by the sequence $I_1, I_{1+q}, I_{1+2q}, \ldots, I_{1+(p-1)q}$. These p current sources are uniformly spaced around the circle.
2) For each input code k, $0 \le k \le N$, the DAC generates p output voltages. Each output voltage is obtained by switching k current sources consecutively starting with one of the p index current sources. Thus, the dth sample $(1 \le d \le p)$ is obtained by switching k current sources starting with $I_{1+(d-1)q}$ and continuing around the circle in the clockwise direction until exactly k current sources have been selected.

This is termed the cyclic DDEM switching sequence. It may appear to be similar to some of the DDFN approaches that are in use, but, in contrast to the DDFN approaches, the cyclic DDEM switching sequence is not data-dependent and is completely deterministic.

Fig. 5 illustrates the cyclic DDEM switching sequence for a 4-bit DAC when the input code is $k = 5$. In this example, $n = 4$, $N = 16$, $p = 4$, and $q = 4$.

Although the cyclic switching sequence does not provide perfectly linear average performance for the DAC output, we will show later that this sequence performs quite well when used for testing of ADCs. At this point, a comparison between the cyclic DDEM switching sequence and the random DEM switching sequence can be made from a hardware implementation viewpoint. It can be shown that the logic needed to implement the cyclic DDEM approach is much simpler than that needed for the random DEM switching sequence. No scrambler is needed in the cyclic DDEM approach and because the index current source values are shifted by a fixed amount, a shift register can be used to drive the switches that select the current sources.

Although the cyclic DDEM switching sequence results in a significant reduction in the number of samples per ADC output code when compared with what is obtained for the natural DDEM switching approach, it must be recognized that the number of current sources and switches is still large when n is large. Some preliminary results focusing on reducing the required number of current sources with DDEM switching sequences can be found in [28]. In the remainder of this paper, we will focus on the performance potential for the DDEM approach for testing of ADCs and on a comparison of the

DDEM approach with the random DEM approach in the same test environment.

C. Random DEM and DDEM Testing of Medium-Resolution ADCs

Simulation results showing the performance potential of using DEM for testing medium-resolution ADCs will be presented in this section. A comparison of the ideal random DEM and the proposed DDEM approaches will also be made. Although we could have compared against any other existing DEM strategies for low-resolution DACs, implementing such strategies even in software becomes a major challenge when the resolution of the DAC becomes high. On the other hand, an ideal randomizer is physically impossible to implement, but it is really easy to implement in simulation. That is why we choose to compare against the ideal random DEM approach.

It will be assumed that the DUT is an R-string flash ADC as described in Fig. 1 and that the signal generator used for testing is a current-steering DAC as described in Fig. 3. The ADC resistors will be modeled as uncorrelated random samples from a truncated Gaussian population with a mean value of $R_0\ \Omega$ and a standard deviation of $0.2R_0\ \Omega$, where R_0 is the nominal value of the resisters. Because realistic resistance values due to random process variations typically follow a Gaussian distribution with the tails truncated, our simulation also uses a truncated Gaussian distribution to generate the resistance values. Any resistance values that are outside the -5 sigma band were discarded and regenerated. It will be assumed that there is no offset voltage in the comparators of the ADC because the comparator offset causes transition point errors that can be lumped into errors in the resistor string. It will also be assumed that the DACs nonlinearity is dominantly due to mismatch in the current sources. To model the mismatch in the current sources, it will be assumed that the current sources come from uncorrelated samples of a truncated Gaussian random variable with a mean of I_0 A and a standard deviation of $0.2I_0$ A, where I_0 is the nominal value of the current sources. As for the resistors, the truncation in the distribution is at the -5 sigma value in the original Gaussian distribution.

The DUT, which is an ADC with 7 bits of resolution, will be tested with a DAC that has 10 bits of resolution. In these simulations, it will be assumed that the output code densities of the DUT are used to calculate the INL_k from the expression

$$\mathrm{INL} \cong \max_{k=1}^{N-1}(\overline{\mathrm{INL}_k}) \tag{5}$$

where $\overline{\mathrm{INL}_k}$ is given by (4).

Figs. 6 and 7 show simulation results for a population of 100 ADCs tested with a single DAC for both random DEM and the cyclic DDEM switching sequences for the DAC. One hundred twenty-eight samples per digital input code to the DAC were used to generate the data in Fig. 6. Eight samples per digital input code to the DAC were used to generate the data in Fig. 7. The DAC was selected as a sample from the population DACs that were generated and had an INL of 10.056 LSB. Although the simulation results presented in these figures were based upon a single DAC from the population and a limited set

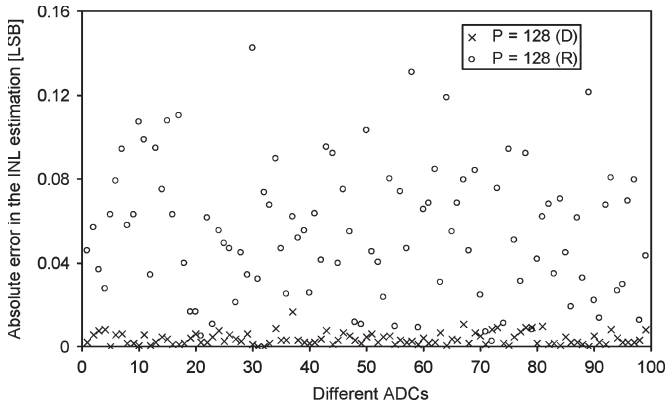

Fig. 6. Comparison of the two methods [random (R) and deterministic (D)] for estimating INL error using 100 different ADCs and $p = 128$.

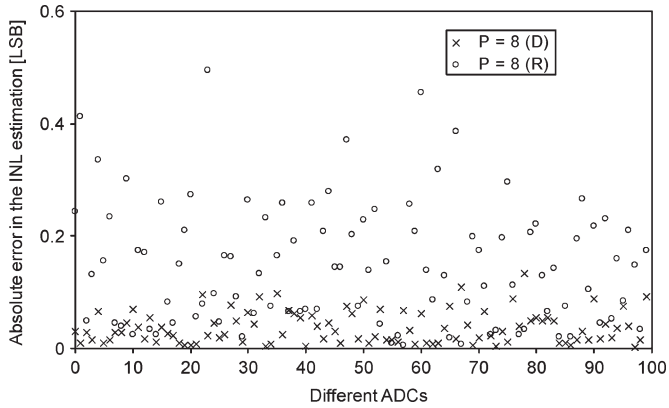

Fig. 7. Comparison of the two methods [random (R) and deterministic (D)] for estimating INL error using 100 different ADCs and $p = 8$.

of 100 DUTs, extensive simulation had been conducted with many different DACs from the sample population and many different sets of ADCs. The results shown in Figs. 6 and 7 are representative of what were obtained in a large number of simulation runs. From these figures, several important observations can be made. First, both the random DEM and the DDEM approaches provide good estimates of the actual INL of the DUT. Second, the fact that the cyclic DDEM switching sequence is not perfectly average linear does not seriously degrade the potential of the DDEM approach. Third, the cyclic DDEM switching sequence offers substantial improvement in testing performance over that of the random DEM approach for a given number of samples using both DAC architectures. Finally, the DDEM approach with p equal to 8 has performance comparable to that of the random DEM approach with p equal to 128. This latter result is particularly important because the substantial reduction in the number samples will directly result in a substantial reduction in testing time when used in either BIST or production test environments.

It should be observed that although the DDEM approach performs very well in the simulation, the cyclic switching sequence is just one of many DDEM switching sequences that can be used. The issue of optimality of the deterministic switching sequence has not been addressed. It should be emphasized that many deterministic switching sequences will give very poor results. It may be the case, however, that other

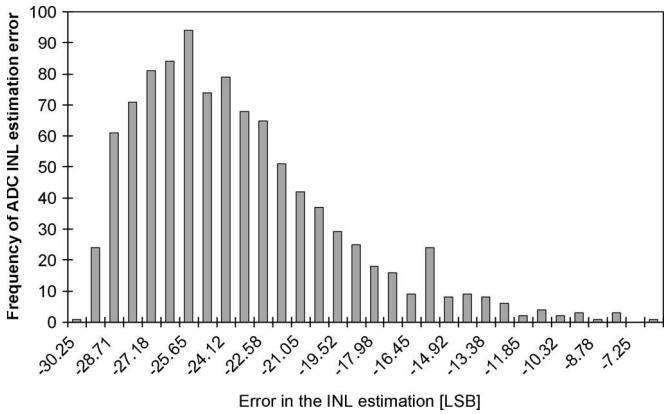

Fig. 8. INL estimation error distribution when testing 1000 different ADCs with no DEM DAC.

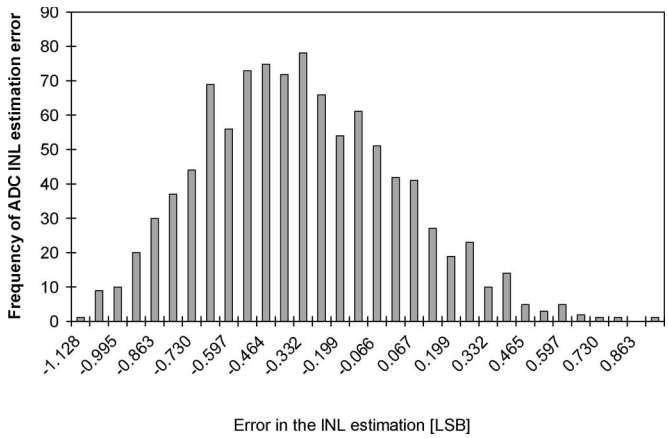

Fig. 9. INL estimation error distribution when testing 1000 different ADCs using a DDEM DAC with $p = 32$.

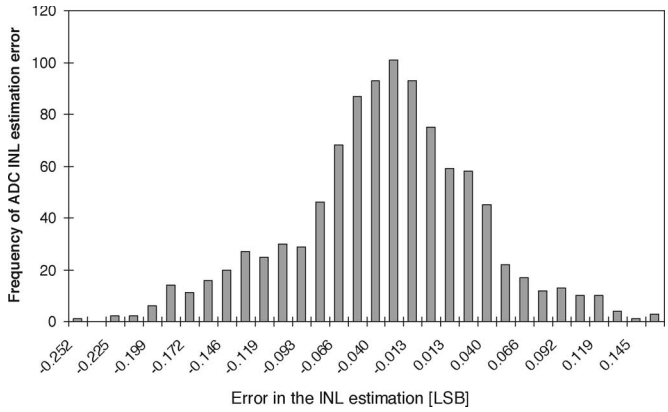

Fig. 10. INL estimation error distribution when testing 1000 different ADCs using a DDEM DAC with $p = 128$.

deterministic switching sequences perform even better than the cyclic approach considered here.

V. DDEM Testing of High-Resolution ADCs

In this section, the use of DDEM DACs for testing high-resolution ADCs will be considered. Although random DEM will also give good performance, the discussion in this section will be limited to DDEM because a much smaller number of samples will be required to obtain a given level of performance.

Using the same model as in the previous section, DACs with 18-bit resolution were used to test 16-bit ADCs using histogram output data. The DAC current sources were generated from uncorrelated samples of a truncated Gaussian random variable with a mean of I_0 A and a standard deviation of $0.2I_0$ A. The resistors in the R-string of the ADC were generated as uncorrelated samples from a truncated Gaussian population with a mean value of R_0 Ω and a standard deviation of $0.03R_0$ Ω. The DAC output range was made 2% bigger than the ADC input voltage range to maintain good uniformity in the input signal at both extremes of the input range. Random noise was added to all DAC outputs to model device noise and measurement errors. The random noise for each output was from random uncorrelated samples of a uniformly distributed random variable with the distribution bounded by ± 3 $\mathrm{LSB}_{\mathrm{DAC}}$.

One thousand ADCs were randomly generated. These ADCs had an average INL of 6.65 LSB with the INL for individual ADCs ranging from 2.5 to 15.7 LSB. A single DAC from the sample population was selected to test these 1000 ADCs. The DAC used for the testing had an INL of 136.5 LSB (34.1 LSB relative to that of the ADC) which corresponds to about 10 bit DAC linearity. Fig. 8 shows the histogram of the INL estimation errors for the 1000 different ADCs when the DAC used for testing has no DEM, but each DAC code is input 128 times to the ADC. It is apparent from this figure that the large INL of the DAC causes large errors in the estimate of the INL of the ADC. Figs. 9 and 10 show how the errors in the INL estimation are reduced with the cyclic DDEM switching sequence for $p = 32$ and $p = 128$ DAC outputs per digital code. The maximum error in INL estimation in this sample of 1000 ADCs is 1.12 LSB with $p = 32$ DAC input codes, and this drops to 0.25 LSB for $p = 128$ DAC input codes. These simulation results suggest that 16-bit ADCs can be tested using DDEM techniques with DACs that are only about 10-bit linear.

The histogram plots for the 1000 samples of Figs. 9 and 10 show little about how accurately the INL_k of the individual ADCs were measured. The plot shown in Fig. 11 shows a comparison of the INL_k estimated by the DDEM algorithm with the actual INL_k for one of the ADCs. This is representative of what was observed for other ADCs in the sample population. The actual and estimated INL_k are in close agreement for all transition points.

The INL of the 1000 ADCs used in the previous simulation were all quite large, and most, if not all, would not pass acceptance criteria for marketable 16-bit ADCs. We thus considered a second set of 1000 ADCs that were generated with a smaller value for the standard deviation of the resistor string values. The standard deviation in the R-string was reduced so that most of the ADCs had an INL of around 0.5 LSB. Thus, this test involves testing ADCs that would be considered good by most manufacturers. The DAC has an INL equal to 88.1 LSB, and the DDEM was based upon $p = 128$ samples per DAC input code. This original DAC is only about 11-bit linear. Simulation results are shown in Fig. 12. It should be apparent from this plot that there is close clustering around the line defined by estimated INL = actual INL + 0.14 LSB. This small testing offset error provides a modestly pessimistic

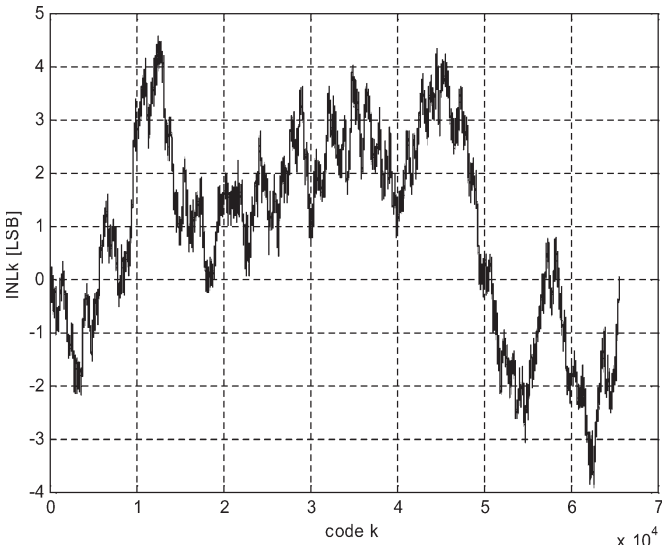

Fig. 11. Estimated and real INL_k for a given ADC using a DDEM DAC with $p = 128$.

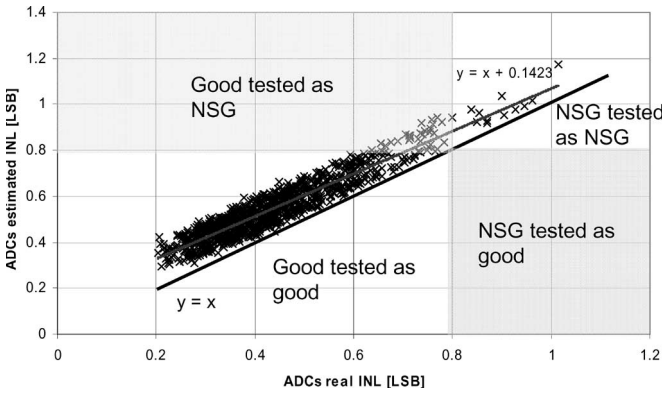

Fig. 12. Testing scheme for 1000 ADCs when using a DDEM DAC with $p = 128$.

estimate of the actual INL. It is important to note, however, that in this sample, no samples lie below the ideal test criteria line defined by estimated INL = actual INL, indicating that the test has not classified any parts to have an INL better than their actual INL. If we define the test acceptance criteria to be devices with a tested (i.e., estimated) INL of at most 0.8 LSB INL and a reduced grade acceptance criteria, termed as "not so good" (NSG), to be devices with tested INL of between 0.8 and 2 LSB, we obtain the classifications of parts indicated in the same figure. We can see in Fig. 12 that although a few good parts are tested as NSG, there are no NSG parts classified as good ones.

We will assume that parts that have INL bigger than 2 LSB are classified as bad parts and should not be shipped to customers. To investigate the effectiveness of the test algorithm of screening defective parts from good parts, we added 10 parts to the sample of size 1000 that had actual INLs near 2 LSB and higher to the population of 1000 mostly good parts. Fig. 13 shows the results of this test. It should be noted that no bad parts are tested as good and that no bad parts are tested as NSG. Furthermore, no good parts were tested as bad and even no NSG parts were tested as good. This slightly pessimistic test will

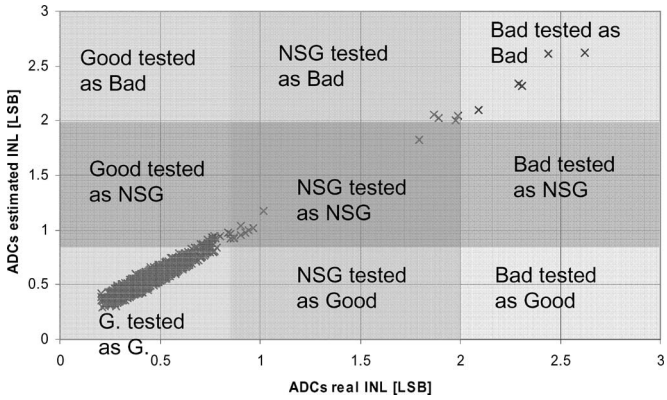

Fig. 13. Testing scheme for 1000 ADCs when using a DDEM DAC with $p = 128$.

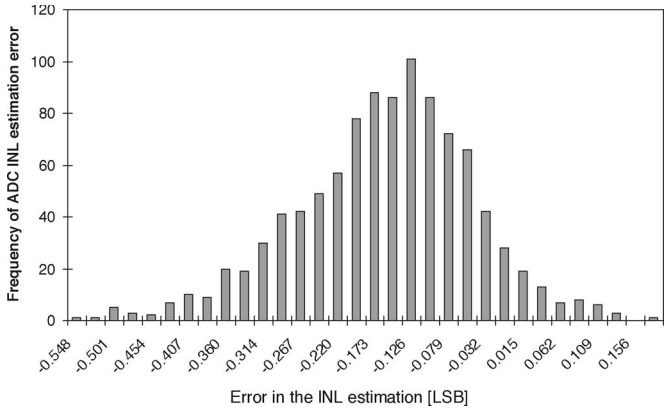

Fig. 14. INL estimation error distribution for 1000 ADC/DAC pairs for $p = 128$.

occasionally move an NSG part with an INL modestly below the bad boundary into the bad classification; it will much more rarely move a bad part near the NSG boundary into the NSG classification, but the probability of moving a good part into the bad category and a bad part into the good category is very small.

The previous simulations focused on using a single DDEM DAC to test a large number of different ADCs. This situation would be common in a production test environment where the excitation source could be part of an ATE system or could be included on the device interface board (DIB) in a tester. In a BIST environment, the DDEM DAC would ideally be fabricated on the same piece of silicon as the DUT. As such, each DUT would have a different DDEM DAC for testing. To address this issue, 1000 ADC/DAC pairs with the cyclic deterministic switching sequence were considered in which the ADCs and the DACs were randomly and independently selected from truncated Gaussian distributions. The standard deviation of the resistors in the R-string was again reduced so that most of the ADCs in the population has an INL of around 0.5 LSB. The 1000 DDEM DACs had 18-bit resolution, and the population had an INL that was, at best, 13-bit linear. Noise was added to each DAC output. The noise was uniformly distributed between -3 and $+3$ LSB of the DAC. Simulation results for the INL estimation are shown in Fig. 14.

From Fig. 14, it should be apparent that the testing results for random ADC/DAC pairs are also quite good with a mean

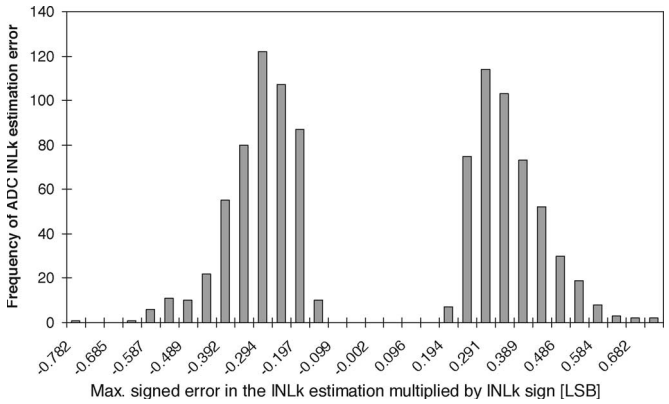

Fig. 15. Histogram of maximum signed INL_k errors multiplied by INL_k sign for 1000 ADC/DAC pairs.

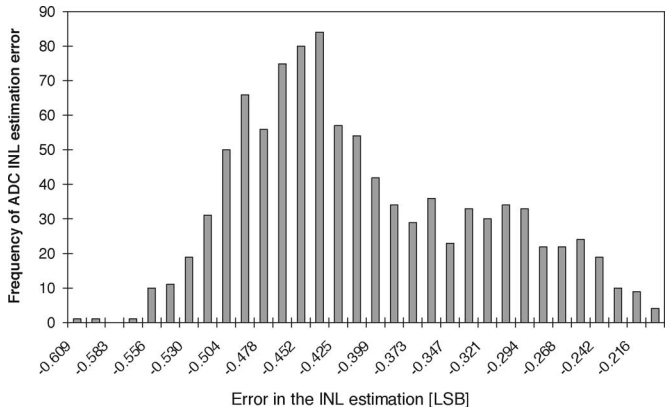

Fig. 16. INL estimation error distribution when testing 1000 different ADCs using a 16-bit DDEM DAC with $p = 128$.

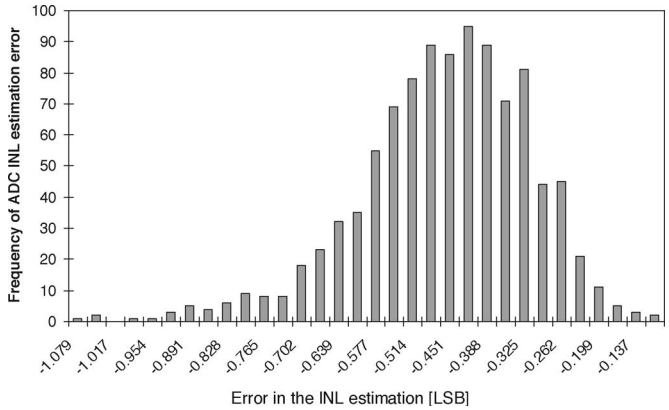

Fig. 17. INL estimation error distribution for 1000 ADC/DAC pairs for $p = 128$.

error of around 0.2 LSB. These results are comparable to what was obtained using a single DDEM DAC to test a population of ADCs.

The INL estimate may differ from the INL_k estimate because the maximum INL deviation will generally differ from where the INL_k estimation error attains a peak value. The INL_k difference is a better indicator of how closely the individual transition points of the ADC can be estimated. Fig. 11 shows how the INL_k estimates related to the actual INL_k for a single ADC/DAC pair. Fig. 15 shows the maximum error in the INL_k estimates multiplied by the sign of the INL_k for the 1000 ADC/DAC pairs used to generate the data of Fig. 14. In Fig. 15, multiplication by the sign of INL_k was used to reflect whether the error was due to an overestimation or an underestimation of the actual INL_k, with a negative result corresponding to an overestimation and a positive result corresponding to an underestimation. From Fig. 15, it is apparent that the underestimates and the overestimates are nearly equally likely to occur.

A comparison of the results in Fig. 15 with those in Fig. 14 shows that the maximum error in the 65 534 INL_k estimates for each pair is modestly larger than the error in the INL estimates, but all INL_k estimates are close to the actual INL_k.

Most existing ADC testing approaches utilize DACs that have higher resolution than the DUT. This is generally considered necessary to avoid the introduction of significant quantization errors. Inasmuch as the linearity of the DDEM DAC can far exceed its resolution, the question of whether the DDEM DAC resolution can be reduced to levels comparable to or possibly even less than the resolution of the DUT deserves attention. We will not provide a detailed investigation of this issue in this paper but will consider the specific situation where the resolution of the DDEM DAC is equal to that of the DUT. Specifically, a 16-bit resolution DAC with 54 LSB INL was used to test the same 1000 16-bit ADCs considered in the previous simulation results. Beyond the reduction in resolution of the DAC, the simulation conditions are the same as before. Fig. 16 shows simulation results for the cyclic switching sequence with $p = 128$. The INL error estimation is mostly less than 0.5 LSB, and using the same test acceptance criteria as before, there are no bad parts that have been identified as good parts. Likewise, no not so good parts are classified as good parts because the INL was modestly overestimated in this simulation.

The application to a BIST environment was considered by using 1000 DDEM DAC/ADC pairs. The DDEM DACs all had 16-bit resolution, and the cyclic deterministic switching sequence was used for the DDEM. As before, the ADCs and DACs were randomly and independently selected from truncated Gaussian distributions. The standard deviation of the resistors in the R-string was again reduced so that most of the ADCs in the population had an INL of around 0.5 LSB. The 1000 DDEM DACs had 16-bit resolution, and the population had an INL that was, at best, 12-bit linear. The same simulation conditions as before were used. The results are shown in Fig. 17.

It should be noted that the testing results for random ADC/DAC pairs shown in Fig. 17 are also quite good, with a mean error of around 0.5 LSB, which are comparable with the results obtained for Fig. 16.

VI. Mathematical Assessment of DDEM Testing Performance

The previous section concentrated on the simulated performance of using DDEM DACs to test both low- and high-resolution ADCs. In this section, we will concentrate on a mathematical formulation of the DDEM testing concept. This

section will formally show that the "averaged DAC" with our DDEM approach can generate a signal that is very close to being an ideal ramp, which means that the DC transfer characteristics of our averaged DAC are very close to being linear. This is done by showing that the INL of the averaged DDEM DAC is very small. It must be stressed here that what we are going to show is much stronger than showing that the expected value of the averaged DAC output is on the fit line, which is guaranteed by construction.

The mismatch in the current sources of the DAC will be modeled by the relationship

$$I_j = I_0(1+\varepsilon_j), \qquad j = 1, \ldots, N \tag{6}$$

where $\varepsilon_j, j = 1, \ldots, N$, are independent and identically distributed Gaussian random variables that model the mismatch in the current sources. Beyond the current source mismatch, it will be assumed that the DACs are ideal. The standard notation for the distribution of ε_j is thus ε_j independent identically distributed (i.i.d.) $\sim N(0, \sigma^2)$, where the standard deviation σ is determined by the area allocated in the design and by process variations.

Inasmuch as one extra current source has been added to the current source array for notational convenience, we will define the fit line to be the line connecting the DAC output voltages corresponding to the first and last DAC thermometer input codes. The first input code corresponds to no current sources being turned on, and the last code corresponds to all N current sources being turned on. The DAC LSB is defined to be the voltage difference between the DAC outputs corresponding to these two codes divided by the number of transitions, N. Inasmuch as the DAC output voltage is assumed to be proportional to the output current of the current source array, we will characterize the linearity of the output current instead of the voltage in all computations. The output current for the input code 0 is 0, and the output current for input code k for $1 \leq k \leq N$ is given by

$$I(k) = \sum_{j=1}^{k} I_j = kI_0 + I_0 \sum_{j=1}^{k} \varepsilon_j. \tag{7}$$

From (7), it follows that the output for code N is given by

$$I(N) = \sum_{j=1}^{k} I_j = NI_0 + I_0 \sum_{j=1}^{N} \varepsilon_j \tag{8}$$

therefore, the LSB of the DAC is given by

$$I_{\mathrm{LSB}} = \frac{I(N)}{N} = I_0 + \frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j. \tag{9}$$

It can be observed that the random variable I_{LSB} is Gaussian with a $N(I_0, (I_0^2/N)\sigma^2)$ distribution. Since N is very large for even modest resolution, the deviation of I_{LSB} from I_0 is very small. The fit line of the DAC for each input code k is then given by

$$I_{\mathrm{FIT}}(k) = kI_{\mathrm{LSB}} = kI_0 + I_0 \frac{k}{N} \sum_{j=1}^{N} \varepsilon_j. \tag{10}$$

It follows that the INL_k for the DAC without using DEM is given by the expression

$$\mathrm{INL}_k = \begin{cases} 0, & k = 0, N \\ I_0 \left(\sum_{j=1}^{k} \varepsilon_j - \frac{k}{N} \sum_{j=1}^{N} \varepsilon_j \right), & 0 < k < N \end{cases}. \tag{11}$$

It follows from (11) that the distribution for the INL_k is [29] $N(0, ((N-k)kI_0^2/N)\sigma^2)$, and the largest standard deviation in INL_k (in LSB) is approximately

$$\sigma_{\mathrm{INL}_k} = \frac{\sqrt{N}}{2}\sigma. \tag{12}$$

The average deviation from the average fit line for the DDEM DAC will now be determined. Because each code is input p times and because it will be assumed that the first and last input codes (codes 0 and N) are also input p times, these codes determine the endpoint fit line. It thus follows that the average fit line is identical to the fit line defined in (10). The average deviation from the average fit line at code k is defined to be the INL_k for the DDEM DAC at code k and is denoted as $\overline{\mathrm{INL}_k}$.

Each of the p inputs for code k in the cyclic switching sequence is given by

$$I_d(k) = \sum_{j=1}^{k} I_{(d-1)q+j}, \qquad d = 1, \ldots, p. \tag{13}$$

The average of the p samples for code k, which is denoted by $\overline{I}(k)$, is given by

$$\overline{I}(k) = \frac{1}{p} \sum_{d=1}^{p} \sum_{j=1}^{k} I_{(d-1)q+j}. \tag{14}$$

It follows from (6), (10), and (14) that

$$\overline{\mathrm{INL}_k} = \overline{I}(k) - I_{\mathrm{FIT}}(k) = \frac{I_0}{p} \sum_{d=1}^{p} \sum_{j=1}^{k} \varepsilon_{(d-1)q+j} - k\frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j. \tag{15}$$

From this simple expression, it can be observed that whenever k is a multiple of q, that is $k = hq$, then (15) can be rewritten as

$$\begin{aligned} \overline{\mathrm{INL}_k} &= \overline{I}(k) - I_{\mathrm{FIT}}(k) \\ &= \frac{hI_0}{p} \sum_{j=1}^{N} \varepsilon_j - hq\frac{I_0}{N} \sum_{j=1}^{N} \varepsilon_j \\ &= hI_0 \left(\frac{1}{p} - \frac{q}{N} \right) \sum_{j=1}^{N} \varepsilon_j. \end{aligned} \tag{16}$$

Hence, the cyclic switching sequence was defined under the assumption that $qp = N$, and it follows that the term in

parenthesis in (16) is zero, and thus, the $\overline{\text{INL}}_k = 0$ whenever k is a multiple of q. This implies the average value of the input for the cyclic switching sequence is exactly on the fit line whenever k is a multiple of q.

We will now derive an expression for the standard deviation of the $\overline{\text{INL}}_k$ when k is not necessarily a multiple of q. The two terms on the right-hand side of (15) contain correlated random variables; thus, the standard deviation is difficult to obtain directly from this equation. If we express $k = tq + s$, then the index k will span the linear space from 0 to N when t and s span the linear space from 0 to $p-1$ and 1 to q, respectively, where we are again assuming that $pq = N$. It follows from (6) and (14) that

$$\overline{\text{INL}}(k) = kI_0 + I_0\frac{1}{p}\left(t\sum_{d=1}^{p}\sum_{j=s+1}^{q}\varepsilon_{(d-1)q+j} + (t+1)\sum_{d=1}^{p}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right). \quad (17)$$

This can be simplified to the expression

$$\overline{\text{INL}}(k) = kI_0 + I_0\frac{1}{p}\left(t\sum_{j=1}^{N}\varepsilon_j + \sum_{d=1}^{p}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right). \quad (18)$$

It thus follows from (10) and (18) that

$$\overline{\text{INL}}_k = I_0\frac{1}{p}\left(t\sum_{j=1}^{N}\varepsilon_j + \sum_{d=1}^{p}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right) - I_0\frac{k}{N}\sum_{j=1}^{N}\varepsilon_j. \quad (19)$$

This can be rewritten as

$$\overline{\text{INL}}_k = I_0\left[\left(\frac{1}{p}-\frac{s}{N}\right)\sum_{d=1}^{p}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j} - \frac{s}{N}\sum_{d=1}^{p}\sum_{j=s+1}^{q}\varepsilon_{(d-1)q+j}\right]. \quad (20)$$

The random variables under the two summands in (20) are now uncorrelated, and thus, it follows that the normalized $\overline{\text{INL}}_k$ normalized to a LSB is a Gaussian random variable characterized by

$$\frac{\overline{\text{INL}}_k}{I_0} \sim N(0, A\sigma^2) \quad (21)$$

where

$$A = \left(\frac{1}{p}-\frac{s}{N}\right)^2 ps + \left(\frac{s}{N}\right)^2 p(q-s) = \frac{s(q-s)}{pq}. \quad (22)$$

It can be shown from (22) that the variance of $\overline{\text{INL}}_k$ reaches a maximum value at $s = q/2$. Using this value for s, it follows that the standard deviation of $\overline{\text{INL}}_k$ in LSB is given by

$$\sigma_{\overline{\text{INL}}_k,\max} = \sqrt{\frac{q}{4p}}\sigma = \sqrt{\frac{N}{4p^2}}\sigma. \quad (23)$$

A comparison of the maximum standard deviation of INL_k for the basic DAC as given in (12) with the $\overline{\text{INL}}_k$ of the DDEM DAC as given in (23) will illustrate the level of reduction achievable with the cyclic switching sequence for the DDEM structure. Consider $n = 18$, $p = 2^7 = 128$, and $q = 2^{11}$. It thus follows that the maximum standard deviation of the cyclic DDEM DAC is $\sqrt{(q/4p)}\sigma = 2\sigma$ LSB, and that of the basic DAC is $(\sqrt{N}/2)\sigma = 2^8\sigma$ LSB. Thus, although the cyclic DDEM DAC is not perfectly linear, it has many points that lie exactly on the fit line, and the standard deviation of the largest variant from the fit line is reduced by a factor of 2^7, as compared with that of the basic DAC.

Inasmuch as $(\sqrt{N}/2)\sigma$ is generally much larger than $\sqrt{(q/4p)}\sigma$, it can be concluded that the average INL of the DDEM DAC ($\overline{\text{INL}}$) will be much smaller than the INL of the basic DAC. Furthermore, because $\overline{\text{INL}}_k$ for the cyclic DDEM DAC is so small even with σ modestly large, the current sources in the DDEM DAC can be built without using large area. For example, if the standard deviation of the current sources is 0.1 LSB, the 18-bit DDEM DAC in the previous example will have a maximum standard deviation of $\overline{\text{INL}}_k$ of only 0.2 LSB, and that of the corresponding $\overline{\text{INL}}$ will be somewhat smaller.

Although we will not present a statistical analysis of testing an ADC with the cyclic switching sequence used in the DDEM DAC, the issue of why the deviation of the average input from the average fit line is a good metric for predicting the performance of the DDEM DAC in a testing application does deserve attention. The performance of these switching sequences was validated by the computer simulations discussed in the previous sections. Mathematically, this performance is obtained because the individual variations of the DAC output current among the p samples for the same DAC input code k can be treated as zero-mean uncorrelated additive noise to the ideal ramp presented at the input of the ADC, and such noise does not bias the measurement of the nonlinearities of the ADC. Furthermore, simple layout techniques are well known in the IC design community that can ensure with high confidence levels that the DAC mismatch errors are uncorrelated and have zero mean.

VII. Summary

In this paper, a method for testing ADCs using both random DEM and DDEM DACs has been presented. It has been shown that the DDEM approach offers a substantial improvement in performance over what is attainable with random DEM structures from a computational efficiency point of view. It has been demonstrated through both computer simulations and a mathematical analysis that with the DDEM testing approach, DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADCs. In addition to the performance improvement, the DDEM excitations require substantial reductions in hardware complexity when compared

with random DEM approaches that require good randomizers. The DDEM technique offers potential for use both in BIST and production test environments because the linearity of the testing signal generator is relaxed and the area required to implement it in silicon is small.

REFERENCES

[1] Semiconductor Industry Association. (2001). *2001 Edition International Technology Roadmap for Semiconductors*. [Online]. Available: http://public.itrs.net/Files/2001ITRS/Home.htm

[2] M. Burns and G. W. Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*. New York: Oxford Univ. Press, 2001.

[3] K. L. Parthasarathy, L. Jin, D. Chen, and R. L. Geiger, "A modified histogram approach for accurate self-characterization of analog-to-digital converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 2, pp. 376–379.

[4] J. Wang, E. Sanchez-Sinencio, and F. Maloberti, "Very linear ramp-generators for high resolution ADC BIST and calibration," in *Proc. 43rd IEEE Midwest Symp. Circuits Syst.*, Aug. 2000, vol. 2, pp. 908–911.

[5] S. Bernard, F. Azais, Y. Bertrand, and M. Renovell, "A high accuracy triangle-wave signal generator for on-chip ADC testing," in *Proc. 7th IEEE Eur. Test Workshop*, May 2002, pp. 89–94.

[6] B. Provost and E. Sanchez-Sinencio, "On-chip ramp generators for mixed-signal BIST and ADC self-test," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 263–273, Feb. 2003.

[7] B. Dufort and G. W. Roberts, "Signal generation using periodic single and multi-bit sigma–delta modulated streams," in *Proc. Int. Test Conf.*, Nov. 1997, pp. 396–405.

[8] M. F. Toner and G. W. Roberts, "A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma–delta ADC," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 43, no. 8, pp. 608–613, Aug. 1996.

[9] K. Arabi and B. Kaminska, "Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits," in *Proc. Int. Test Conf.*, Nov. 1997, pp. 786–795.

[10] F. Azaz, S. Bernard, Y. Bertrand, and M. Renovell, "Towards an ADC BIST scheme using the histogram test technique," in *Proc. 5th IEEE Eur. Test Workshop*, May 2000, pp. 53–58.

[11] R. de Vries, T. Zwemstra, E. Bruls, and P. Regtien, "Built-in self-test methodology for A/D converters," in *Proc. Eur. Des. Test Conf.*, Mar. 1997, pp. 353–358.

[12] L. Jin, K. L. Parthasarathy, D. Chen, and R. L. Geiger, "A blind identification approach to digital calibration of analog-to-digital converters for built-in-self-test," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 2, pp. 788–791.

[13] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen, and R. L. Geiger, "Linearity testing of precision analog-to-digital converters using stationary nonlinear inputs," in *Proc. Int. Test Conf.*, Sep. 2003, pp. 218–227.

[14] K. Parthasarathy, T. Kuyel, D. Price, L. Jin, D. Chen, and R. L. Geiger, "BIST and production testing of ADCs using imprecise stimulus," *ACM Trans. Des. Automat. Electron. Syst.*, vol. 8, no. 4, pp. 522–545, Oct. 2003.

[15] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. Hoboken, NJ: Wiley, 1997.

[16] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 6, pp. 795–800, Dec. 1976.

[17] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 267–273, Apr. 1989.

[18] H. T. Jensen and I. Galton, "A low-complexity dynamic element matching DAC for direct digital synthesis," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 1, pp. 13–27, Jan. 1998.

[19] ——, "An analysis of the partial randomization dynamic element matching technique," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 12, pp. 1538–1549, Dec. 1998.

[20] B. H. Leung and S. Sutarja, "Multibit $\sigma-\delta$ A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 1, pp. 35–51, Jan. 1992.

[21] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\sigma-\delta$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[22] R. W. Adams and T. W. Kwan, "Data-directed scrambler for multi-bit noise shaping D/A converters," U.S. Patent 5 404 142, Apr. 4, 1995.

[23] D. Cini, C. Samori, and A. L. Lacaita, "Double-index averaging: A novel technique for dynamic element matching in $\sigma-\delta$ A/D converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 4, pp. 353–358, Apr. 1999.

[24] R. E. Radke, A. Eshraghi, and T. S. Fiez, "A 14-bit current-mode $\sigma-\delta$ DAC based upon rotated data weighted averaging," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1074–1084, Aug. 2000.

[25] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S.-L. Chan, "A 90-db SNR 2.5-mhz output-rate ADC using cascaded multibit delta–sigma modulation at $8\times$ oversampling ratio," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820–1828, Dec. 2000.

[26] U. G. P. M. F. M. V. Ferragina, A. Fornasari, and L. Monfasani, "Use of dynamic element matching in a multi-path sigma–delta modulator," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2004, vol. 1, pp. 649–652.

[27] R. S. S. R. Norsworthy and G. C. Temes, *Delta–Sigma Data Converters: Theory, Design and Simulation*. Piscataway, NJ: IEEE Press, 1997.

[28] B. Olleta, "Precise linear signal generation with nonideal components and deterministic dynamic element matching," M.S. thesis, Dept. Elect. Comput. Eng., Iowa State Univ., Ames, 2003.

[29] Y. Cong and R. L. Geiger, "Formulation of INL and DNL yield estimation in current-steering d/a converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2002, vol. 3, pp. 26–29.

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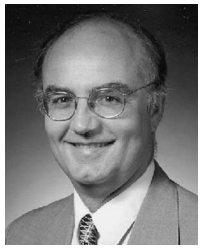

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